

Exhibit B

of

37 C.F.R. § 1.131 Declaration

of Alan L. Lasneski

REGISTERS TO DETERMINE MODE

MAC

- 1.) LINE CNT
- 2.) CLOCK CNT
- 3.) CLOCK CNT CONTROL (ONE TIME PROGRAMMABLE REG.)
- 4.) VIDEO STATUS REGISTER

REGISTERS TO WRITE A MODE

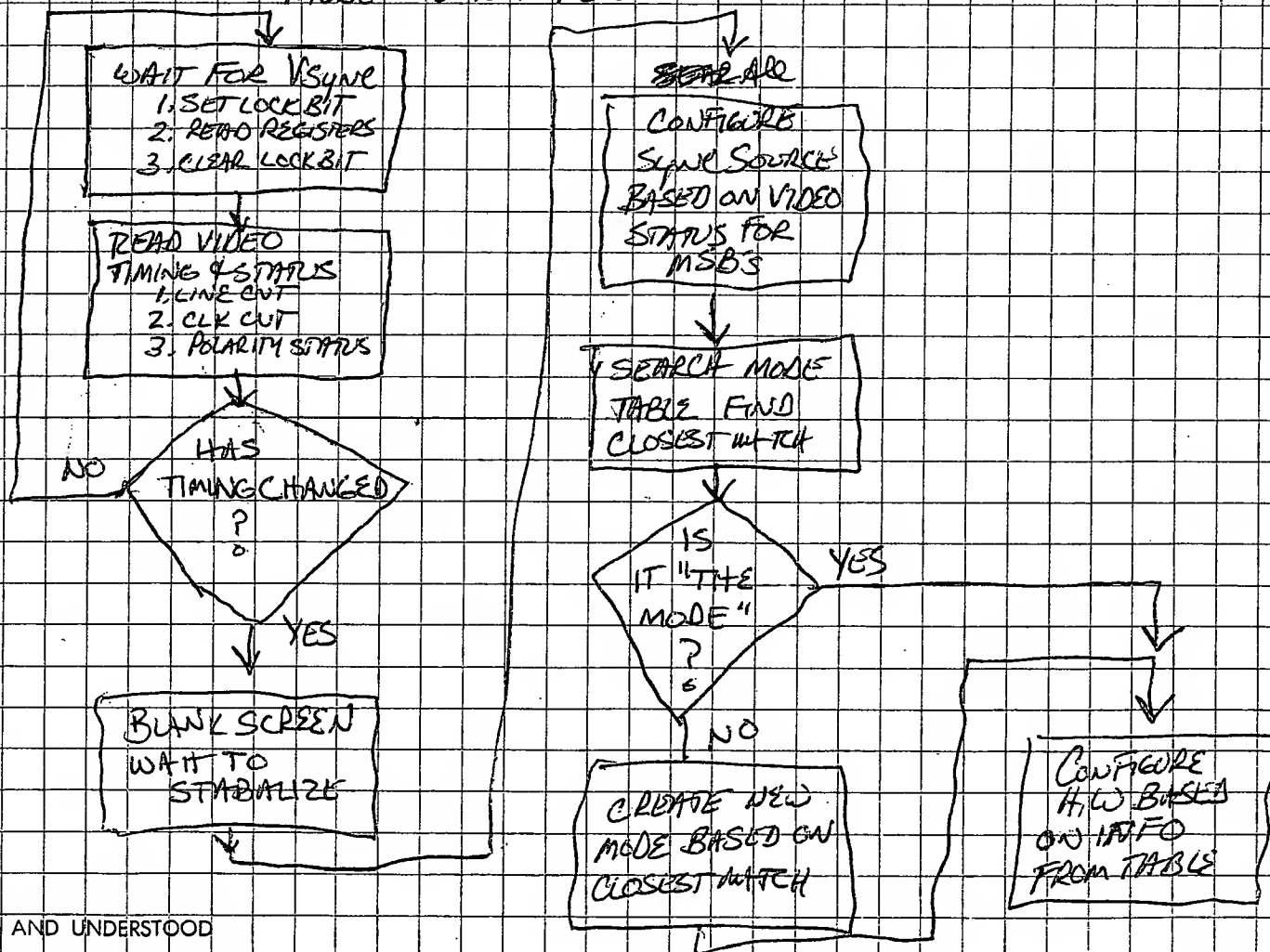
MID

- 1.) CLOCKS PER LINE
- 2.) CLOCK CONTROL REG.
- (3.) COAST START STOP

MAC

1. CAPTURE CONTROL

MODE DETECT FLOW



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ITEMS IN MODE TABLE:

INPUTS:

1. CLK CNT
2. LINE CNT
3. VERTICAL POLARITY > 3 STATES
4. HORIZONTAL POLARITY > 1, 0, IGNORE
5. VERTICAL RESOLUTION
6. HORIZONTAL RESOLUTION

OUTPUTS:

- 1.) CLOCKS PER LINE
- 2.) CONFIGURE SYNC SOURCE
- 3.) PLL CONFIGURATION!
 - a.) PROGRAMMING Δ BASED ON VIDEO MODE
 - b.) USE INDEX INTO PLL TABLE FOR PREG.

STATUS:

VPOS > WHAT WAS LAST USED FOR
HPOS > THIS MODE.

NOTES:

1. FOR NOW LEFT JUSTIFY EVERYTHING
2. CONSTANTLY READING THE POSITION REGISTER FROM POWER ON.
3. IF NO VIDEO DETECTED.
 1. MEM FREEZE BIT SHOULD BE SET.
 2. PLL SHOULD BE DISABLED \rightarrow TO SAVE MERLIN
 3. BLANK THE SCREEN (OR SOLID BLUE) OR SOME COLOR
4. HAVE 2 CARDS NEED TO SAVE MODE INFO FOR EACH CARD.
 1. SO CAN SWITCH MODES AND USE UNIQUE VALUES TO THAT DEVICE. (BRIGHTNESS ETC.)
5. IF DETECT MODE SWITCH MAKE LCD GO BLACK - SO CUSTOMER DOES NOT SEE SCREEN STRETCH OR OTHER.
 1. SET LCD CLR BIT
 2. WAIT FOR NEW MODE TO STABILIZE
 3. THEN CONTINUE -
- 6.) IF INTERLACE BIT IS SET THEN SET INTERLACE ENABLE BIT. (IN MISC CONTROL REG.)

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A) WHAT DETERMINES A VIDEO CHANGE?

- 1.) CHECK SYNC SOURCE TABLE FOR CHANGE ON MSB'S
- 2.) LINE CNT REG CHANGE BY MORE THAN 1.
- 3.) CLK CNT. - SET A RANGE IN WHICH IT CAN VARY FROM CURRENT VALUE. START WITH ± 4 . RECHECK AND UPDATE VALUE CONSTANTLY.
- 4.) IF VPOL OR HPOL HAVE CHANGED FROM LAST SETTINGS AND THE MODE TABLE DOES NOT SAY IGNORE!

B.) IF DETERMINE ITS TIME TO SWITCH:

- 1.) WAIT FOR VALUES TO STABILIZE.
 - A.) THE VALUES CAN CHANGE ONLY EVERY VSYNC.
 - B.) CHECK HSTATUS BITS (MSB'S) CLK CNT, LINE CNT.
- 2.) WHAT DOES STABILIZE MEAN?
 - A.) CONSTANT OVER SOME PERIOD OF TIME
 - B.) LAST N VSYNCS WITHIN TOLERANCE OF ABOVE SET VALUES. IF NOT RESET COUNTER.

C.) NOW STABILIZE SEARCH THE TABLE.

- 1.) FIND ONE WITH CLOSEST LINE CNT & CLOSEST CLOCK CNT.
 - a.) ALGORITHM FOR NOW:

ADD THE DIFFERENCE BETWEEN THE CLOCK CNT DIFFERENCES
ADD THE DIFFERENCE BETWEEN THE LINE CNT (OLD V.S. NEW VALUES)
ONE WITH SMALLEST Δ WINS.
 - b.) THIS MAY CHANGE AS WE LEARN.
- 2.) ~~IF~~ FOR A MATCH LINE CNT CANNOT VARY BY MORE THAN 1
AND CLK CNT MORE THAN SOME VARIABLE AMOUNT START WITH ± 4 COUNTS.

D.) IF NO MATCH.

- 1.) THEN BASE NEW MODE ON CLOSEST MATCH. COPY EVERYTHING BUT CLK CNT & LINE CNT. AND ASSUME SAME VALUES FOR STARTING.

E.) NOW SET THE MODE.

1. AFTER SET SYNC SELECT BIT WAIT A Vsync Cycle.
2. SET CLOCKS PER LINE
3. SET THE PLL VALUES.

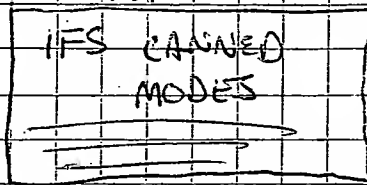
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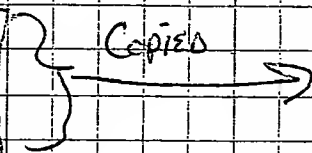
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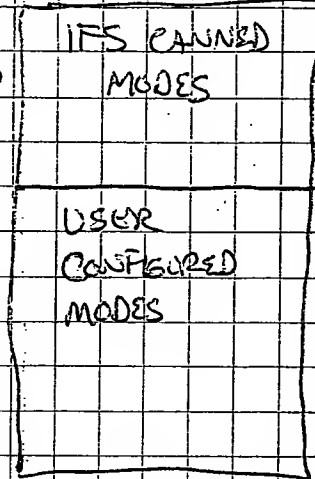
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MODE TABLE
FLASH

COPIED



RAM



CONTROL OF SYNC SOURCE:

INPUTS

OUTPUTS

VoVs	NoHs	NoCs	NoSec	Sync Ser	MemFr2	STATE
0	0	0	0	00	0	
0	0	0	1	00	0	
0	0	1	0	00	0	
0	0	1	1	00	0	
0	1	0	0	01	0	
0	1	0	1	01	0	
0	1	1	0	10	0	
0	1	1	1	00	1	No Video
1	0	0	0	01	0	
1	0	0	1	01	0	
1	0	1	0	11	0	
1	0	1	1	11	0	
1	1	0	0	01	0	
1	1	0	1	01	0	
1	1	1	0	10	0	
1	1	1	1	00	1	No Video

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Inputs

1. a) LEFT
b) RIGHT
2. a) DIGITAL
b) MISS CNT REG.

Outputs

1. a) DELAY line \leftarrow 30. NUTS PER FRAME \leftarrow Adjust Phase
b) CLOCKS PER LINE \leftarrow Adjust Tracking
2. a) DIGITAL FILTER BIT
b) THRESHOLD REGISTER \leftarrow on time setup
c) RGB Select

Base Algorithm:

TRACKING MUST BE SET FIRST THEN PHASE

- 0) WAIT FOR Vsync
- 1) SET PHASE \leftarrow 30. NUTS BUS (DETERMINE)
- 2) WAIT 2 Vsync
- 3) CHECK INFORMATION \rightarrow
- 4) CONFIGURE H/W.

BASIC Phase First

THIS Algorithm works when image fills THE SCREEN.

TWO LEVELS OF DONENESS -

- 1.) I'm done shut algorithm off
- 2.) I'm close enough so unfreeze memory.

$$WIDTH = (R - L + 1)$$

This process will unfreeze memory.

START WITH THIS:

NEED 5 OF THESE IN A ROW \rightarrow
THEN PICK THE MIDDLE CASE

LATER:

MAYBE BUILD A TREE MODEL
THEN PICK THE SCORST SPOT.

- 0.) if screen \neq BLACK then
 - 1.) READ LEFT & RIGHT REGS.
 - 2.) CALCULATE IMAGE WIDTH
 - 3.) IF WIDTH $>$ mode.hres AND WIDTH $<$ mode.hres + 2 THEN PHASE IS BAD!
 - 4.) ELSE IF WIDTH \geq mode.hres + 2 THEN TRACKING IS BAD. (WORK ON THIS LATER)
 - 5.) ELSE IF WIDTH $=$ mode.hres THEN SYNC & TRACKING = OK
 - 6.) ELSE IF WIDTH $<$ mode.hres THEN (PATHOLOGICAL CASE)
 - 1.) PHASE OR TRACKING IS WRONG
 - 2.) OR IMAGE IS NOT FULLY THERE. (WORK ON THIS LATER)

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TO DETERMINE IF BLACK SCREEN:

FOR NOW SET RGB = 0

IF BLACK AND WHITE OR WHITE AND BLACK ARE DIFFERENT
THEN ITS NOT BLACK.

How To Determine pixel clock period.

1. HAVE CLK CNT REG = # of 50MHz clocks over 20 lines. (CNT INTERLINE REG.)

2 CLKS PER LINE (TRACKING)

$$\text{CLKS PER LINE} \times 20 = \# \text{ of pixel clocks in 20 lines}$$

$$\left(\frac{\text{PERIOD OF 20 LINES} = \text{CLK CNT} \times \frac{1}{50 \times 10^6}}{(\text{CLKS PER LINE} \times 20)} \right) = \text{Pixel Frequency}$$

$$\text{Pixel period} = P_{\text{PERIOD}} = \frac{\text{CLK CNT}}{\text{CLKS PER LINE} \times 10^9} = \frac{\text{CLK CNT}}{\text{CLKS PER LINE}} \cdot \text{NANO SECONDS.}$$

← READ FROM CNT
← READ FROM MODE TABLE

EX VGA CLK CNT 31728 = 39.72 nS = 25.175 MHz.

Clock rate 800
CONSTANT

IF STEP DELAY = 25 nS (4,200)

MAX DELAY SETTING = $\left(\text{PIX PERIOD} \times \text{STEP DELAY} \right) \text{ (ROUND UP)}$

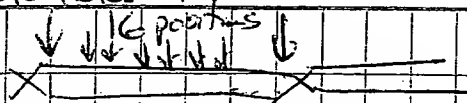
PHASE ADJUST INCREMENT = $\frac{\text{MAX DELAY SETTING}}{16} \leftarrow \text{SAC CONSTANT. (USE 20 INSTEAD.)}$

THEN RUN SEQUENCE LOOKING FOR 5 OR SOME CONSTANT GOOD VALUES
THEN PICK THE MIDDLE ONE.

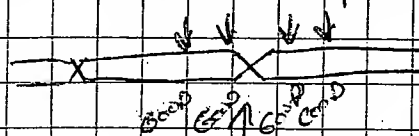
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But could be a problem i.e.



THAT THIS WOULD BE THE MIDDLE BUT IT IS A PROBLEM
SO MAYBE NARROW IN THESE AGAIN?

IF PHASE ADJUSTING * STEP DELAY >

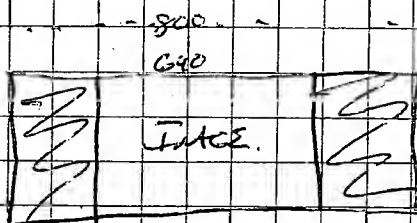
Jitter of 2NS.

↳ 1

THRESHOLD REGISTER. → PRK QW20 FOR NOW.

IT NEEDS TO BE SET BEFORE READING LEFT AND RIGHT REGISTERS.

Auto TRACKING - (ASSUMES A LARGE IMAGE).



EXPECTED WIDTH
ACTUAL WIDTH

HOW MANY PIXELS OFF = ABS(Actual Width - Expected Width)

HORIZONTAL PERIOD
IMAGE PERIOD

(NEW) CLK per line = CLKs PER LINE * $\frac{\text{EXPECTED WIDTH}}{\text{ACTUAL WIDTH}}$ ← KEEP THIS # EVEN.

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PATHOLOGICAL SITUATIONS

IF MODE CHANGES

TRACK_OK = FALSE

THEN

if width > HRES and width < HRES + 2

PHASE IS BAD

TRACK_OK = TRUE

else if width >= HRES + 2

if (TRACK_OK == TRUE)

// TRACKING IS BAD

SET PHASE BAD CHECK NEXT PHASE

else if width == HRES

TRACK_OK = TRUE

else pathological case phase

if (TRACK_OK == TRUE)

SET PHASE BAD CHECK NEXT PHASE

if Sync Select bits change then need to enter new mode!
CHECK TO MAKE SUREif Sync Select changes need to blank screen and force new mode
detect

THEN SET

PATHOLOGICAL CASE NOT ENTERED == TRUE

SO WAIT FOR ⁽⁶⁰⁾ PATHOLOGICAL CNTS BEFORE START
DOING ANYTHING IN THE PATHOLOGICAL CASEIF ALL PHASES ARE BAD PICK ZERO PHASE POSITION. IF TRACK WAS OK.
MEANING LZ ENTERED PHASE IS BAD EVERY SINGLE
TIME

OR SWITCH OVER TO OTHER METHOD. (CAPTURE COMPARE)

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2 conditions under pathological case.

if width > HRES * .95 ^(5%) THEN
ADJUST TRACKING

ELSE

INCREASE PATHOLOGICAL COUNT

if (PATH CNT > LIMIT) THEN:
(60)

★ DON'T MISS WITH TRACKING FOR GO VSYNCS
BOTH CASES PATHOLOGICAL & TRACK IS BAD CASES

NO!

1. SET LCD BLANK
2. WAIT FOR VSYNC
3. FREEZE MEMORY

1. SET LCD BLANK = TRUE
2. UNFREEZE MEMORY
3. WAIT 2 VSYNCS
4. SET DIG FILTER = TRUE
5. WAIT FOR VSYNC
6. READ MISS COUNT (LOCKED)
7. if MISS COUNT < MAX MISSES
TRACK_OK = TRUE

THIS WILL
MOVE TO
ANOTHER
ALGORITHM
NOT INCORPORATED
ANYMORE.

IF INTERR IS TOO SMALL OR CAN'T FIND A GOOD SYNC → THEN USE OLD TABLE TRACK VALUE

★ DON'T MODIFY MODETABLE TRACKING UNTIL YOU KNOW IT'S A CLEAN GOOD SWITCH. KEEP IN A TEMP LOCATION UNTIL KNOWN GOOD! CHANGE CURRENT METHOD USED WHICH MODIFIES THE TABLE

ELSE! USE OTHER ALGORITHM.

IF NO GOOD PHASE RESTORE TRACKING TO ORIGINAL TABLE VALUE
AND ENABLE OTHER ALGORITHM

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M-200 TABLE

ADD NEW ENTRY

* New

ORIGINAL
TRACKINGMODIFIED
TRACKING

USE MODIFIED FIRST IF NON-ZERO THEN SWITCH TO
ORIGINAL TRACKING THEN USE CALCULATED MEAN
AND PLACE INTO MODIFIED TRACKING

4
3 CASES TO ADDRESS

1. Can't Find A Good Phase Set

→ 2 cases

2. image width $< 95\%$ of actual width
& image is not full screen.

→ NEW
ALGORITHM.

3. image width $<$ expected width

& $> 95\%$ & image is not full screen.

→ 1 case

4. fallout of 3 case

Set Sync & Track

and now image is greater than it should be
but mode has not changed.

→ 1 case

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OUT IN MAIN NOT PART OF EXECUTING AUTO PHASE DO THIS:

1. IF width \geq HRES ± 2
expected

THEN

RERUN AUTO PHASE, IF AUTO PHASE IS ALREADY RUN

2. if Auto phase found All Bad Phases

& width $<$ HRES ~~when~~ AUTO WAS RUN

~~IF~~ THEN &

width increases $> * HRES$ THEN Run Auto Phase

CAPTURE COMPARE.

LOOP.

DigFilter = 0

Set Phase

Wait 2 Vsync's

DigFilter = 1

Wait 1 Vsync (100)

if miss cnt $>$ MAX MISSES

Set Bad phase

else

set Good Phase

WHILE DRIVE THIS
IF HRES ~~CHANGES~~ $>$ HRES
WIDTH $>$ HRES
THEN RUN THE OTHER
AUTO PHASE Algorithm
AGAIN.

DigFilter = 0

FIND Good Phases

1. Pick middle one

2. if no good phases

Then go to #2 ABOVE THEN USE CAPTURED VALUES
FOR TRACKING ETC.

★ 1. When using the Capture Control
Set the threshold to 0×10

★ 2. When using the Auto Phase (Normal)
Set the threshold back to normal value currently 0×20

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is no good setting in ^{new} Auto Phase and done
but there are no good positions. THEN
1. RESET TRACKING TO TABLE VALUE CAPTURED
2. RUN CAPTURE COMMAND

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